REMARKS

Applicants respectfully traverse the objections and rejections provided in the Office Action mailed December 20, 2005 (hereinafter "Office Action") for at least the reasons discussed below.

Claims 1-38 are not indefinite

Claims 1-38 stand rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite. In particular, the Office Action objects to the phrase "respect to a reference voltage responsive to a relationship among phase components associated with the polyphase AC output," and asks "what is the relationship among phase components?" Office Action, p. 2.

Applicants submit that this claim language is amply supported by the disclosure of the application as filed. With respect to the "reference voltage," a discussion of an example of such a reference voltage is provided on page 6:

> A power conversion apparatus 300 according to some embodiments of the invention illustrated is illustrated in FIG. 3. In particular, the apparatus 300 includes a DC source 310 (e.g., a battery, rectifier, or other source) operative to generate first and second DC voltages V^+, V^- on a DC link including first and second DC voltage busses 315a, 315b. The apparatus 300 further includes a polyphase DC to AC converter circuit, *e.g.*, an inverter circuit 320, operative to generate a polyphase AC output 325 from the DC voltages V^+, V^- on the DC busses 315a, 315b. ***The apparatus 300 further includes a DC range shifting control circuit 330 operative to shift a range of voltages V^+, V^- on the DC voltage busses 315a, 315b with respect to a reference voltage, for example, a neutral voltage for the AC output 325. In particular, the DC range shifting control circuit 330 is operative to shift the range of voltage between the DC voltage busses 315a, 315b responsive to a relationship among phase components of the AC output 325.***
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> It will be appreciated that the apparatus 300 may be implemented in a number of different ways and/or employed in any number of different applications. For example, the configuration illustrated in FIG. 3 is applicable to power conversion circuitry in both double conversion and line interactive UPSs. In such applications, ***the reference voltage used for the DC range shifting control circuit may be, for example, an actual load neutral (in "Y" connected output configurations) or a "synthetic" neutral computed from line-to-line voltages (in "delta" output configurations)***, and the DC range shifting control circuit 330 may be used to shift the voltage range spanned by the DC voltage busses 315a, 315b about the neutral

(actual or synthetic). As described in further detail below, such a technique may be used to improve conversion efficiency and/or reduce switching component stress.

An example of shifting "a voltage range . . . responsive to a relationship among phase components associated with the polyphase AC output," is described beginning on page 9, line 9 of the specification:

> ***Some embodiments of the invention arise from a realization that creating both a DC voltage reference for regulation of the DC voltage (V^+-V^-) between the first and second DC voltage busses 530a, 530b and a "zero sequence" reference for regulation of the phase voltages at the AC output 502 to provide a shifting or modulation of the range spanned by the DC voltages V^+, V^- with respect to the AC output neutral that can improve conversion efficiency and/or reduce voltage stress.*** Referring to FIG. 6, the control circuit 550 may determine maximum voltage and the minimum phase voltages (e.g., instantaneous or near-instantaneous voltages) among the phase voltages of the input phases A_{in}, B_{in}, C_{in} and the output phases A_{out}, B_{out}, C_{out} (block 610). The phase voltage information for the output phases A_{out}, B_{out}, C_{out} may be obtained by directly sampling (*e.g.*, using an analog to digital converter) the phase voltages and/or by using reference voltage vectors used to produce the output phase voltages. The difference between the minimum and maximum phase voltages may be used to generate a voltage reference for regulating the DC voltage (V^+-V^-) between the DC busses, *i.e.*, such that the magnitude of the DC voltage (V^+-V^-) is at least as great as the magnitude of the difference between the minimum and maximum phase voltages (blocks 620, 630). This DC voltage reference may be peak filtered (*i.e.*, averaged over time).
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> ***The average of the minimum and maximum phase voltages may be used to generate a zero sequence (common mode) reference that is used to regulate the DC bus voltages V^+ and V^- with respect to the neutral N, i.e., the zero sequence reference may be used as a reference vector that may be added to the other reference vectors for regulating the output phases A_{out}, B_{out}, C_{out} (blocks 640, 650). In this manner, the relative magnitudes of the DC voltages V^+, V^- can be maintained substantially in proportion to the relative magnitudes of the minimum and maximum phase voltages. It will be understood that the zero sequence reference may be such that one pole of a polyphase converter need not switch (discontinuous modulation).***

Thus, in the example described, a relationship among output phase voltages (i.e., examples of "phase components") may be used to generate a zero-sequence reference (for example, a reference input for a controller as shown in FIG. 7) to shift the range of the DC bus voltages with respect to the neutral.

In light of the foregoing, Applicants submit that Claims 1-38 are not indefinite.

Claims 1-38 are patentable over Severinsky

Claims 1-38 stand rejected under 35 U.S.C. 102 as being allegedly anticipated by Severinsky. In rejecting these claims, the Office Action merely states that the claims are "clearly anticipated" and cites only FIG. 2 and column 2, lines 59-68 of Severinsky. Applicants submit that this is insufficient evidence to support the rejections. Moreover, the material cited actually underlines why Severinsky clearly does not anticipate the claims.

In particular, the cited passage from column 2 discusses a converter "symmetrical in construction in regards to a common conductor which is connected to the input common conductor-neutral when it is available." Referring to the description of operation of the circuitry in FIG. 1 in columns 6 and 7, "symmetrical" operation entails the switches C are controlled by the control circuit shown in FIG. 2 such that the DC link capacitors 96, 97 have the same voltage. As further explained at column 7, lines 20-31, voltages on the DC link capacitors are constrained to be symmetrical, i.e., the ***range*** between the positive and negative DC rails 94, 95 (see Severinsky, FIG. 1) with respect to the neutral conductor ***is prevented from shifting*** with respect to the neutral conductor. Moreover, the control circuit shown in the cited FIG. 2 operates responsive to ***input*** phase voltages, not a relationship among phase components of a polyphase AC ***output***. See Severinsky, column 5, lines 59-68. Accordingly, the cited material clearly does not disclose or suggest, for example, "a control circuit operatively associated with the polyphase DC to AC converter circuit and configured to shift a voltage range of the first and second DC voltage busses with respect to a reference voltage responsive to a relationship among phase components associated with the polyphase AC output," as recited in independent Claim 1, or corresponding recitations of independent Claims 20 and 29.

For at least the foregoing reasons, Applicants submit that independent Claims 1, 20 and 29, and the claims depending therefrom, are patentable. Applicants further submit that several of the dependent claims are separately patentable, but defer further discussion of these, as the Office Action does not provide any specific indication as to where Severinsky allegedly discloses or suggests the specific recitations of these claims. If the rejections are maintained in a subsequent office action, Applicants respectfully request that the Examiner

specifically indicate where Severinsky or the other art of record discloses or suggest that specific recitations of the claims, and that the rejection not be made final to afford Applicants the opportunity to address the specific allegations.

Conclusion

Applicants respectfully request withdrawal of the rejections in the Office Action for at least the reasons discussed above. Applicants submit that the claims are in condition for allowance, and request allowance of the claims and passing of the application to issue in due course. Applicants encourage the Examiner to contact the undersigned by telephone to resolve any remaining issues.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on March 20, 2006.

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